COFC/A

Attorney's Docket No.: 09464-010001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RTC

#23
JW

Applicant : Marco Zuniga et al.
Patent No. : 6,400,126 B1
Issue Date : June 4, 2002
Serial No. : 09/475,713
Filed : December 30, 1999
Title : SWITCHING REGULATOR WITH MULTIPLE POWER TRANSISTOR DRIVING VOLTAGES

Art Unit : 2838
Examiner : Shawn Riley

Certificate
MAY 0 8 2003
of Correction

Certificate of Correction Branch
Commissioner for Patents
Washington, DC 20231

TRANSMITTAL OF REQUEST FOR CERTIFICATE OF CORRECTION

Applicant hereby requests that a certificate of correction be issued for the above patent in accordance with the attached request.

One or more of the errors sought to be corrected were made by applicant and a check for $100 is enclosed to cover the required fee of 37 CFR §1.20(a).

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 4/25/03

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CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

April 25, 2003
Date of Deposit

Signature

Sally Zumba.
Typed or Printed Name of Person Signing Certificate

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,400,126 B1

DATED : JUNE 4, 2002

INVENTOR(S) : MARCO A. ZUNIGA AND CHARLES NICKEL

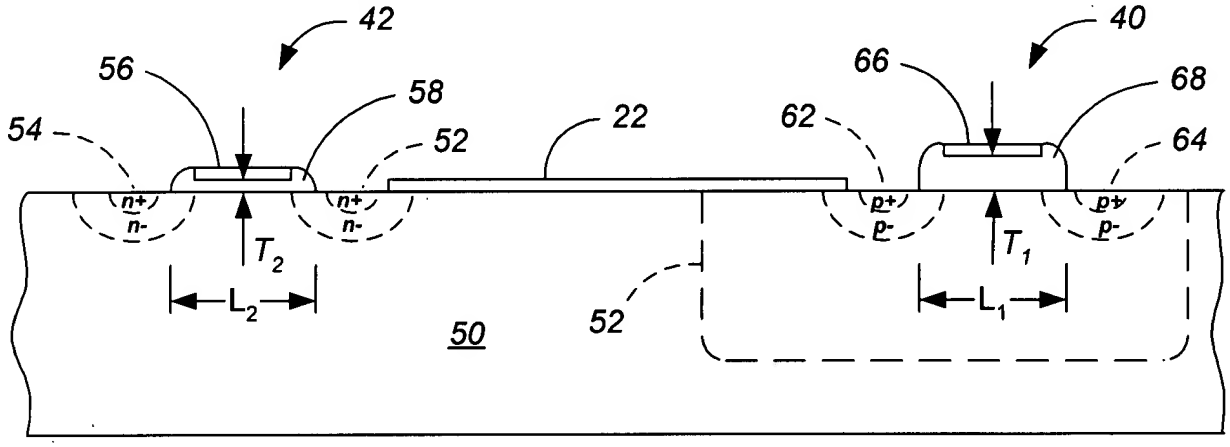
It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 6, line 19, change "PMOS transistor 40" to --NMOS transistor 42--; line 22, change "NMOS" to --PMOS--; line 26 change "PMOS" to --NMOS--; line 30, change "T_2" to --T_1--; line 31, change "68" to --58--; and line 32, change "T_1" to --T_2-- and change "58" to --68--.

In claim 14, line 1, after "first" insert --gate--; line 2, after "second" insert --gate--.

In Sheet 1 of the drawings, FIG._1, element 40 should show a PMOS symbol and element 42 should show an NMOS symbol.

In Sheet 1 of the drawings, FIG._4 should appear as follows:



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PATENT NO. 6,400,126 B1

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

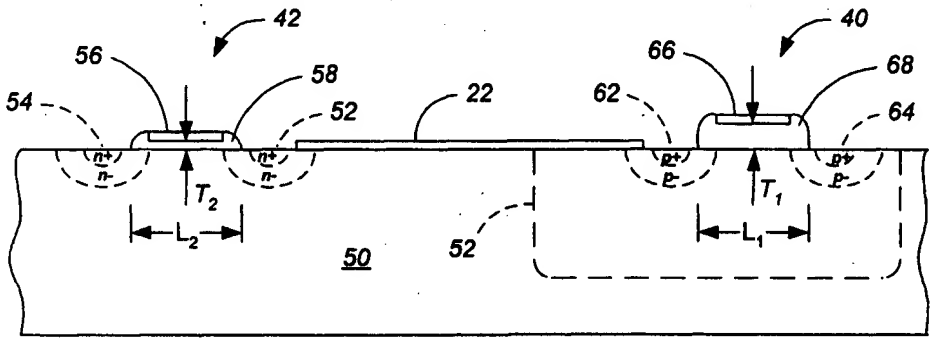
PATENT NO. : 6,400,126 B1
DATED : June 4, 2002
INVENTOR(S) : Marco A. Zuniga and Charles Nickel

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6,
Line 19, change "PMOS transistor 40" to -- NMOS transistor 42 --;
Line 22, change "NMOS" to -- PMOS --;
Line 26, change "PMOS" to -- NMOS --;
Line 30, change "T_2" to -- T_1 --;
Line 31, change "68" to -- 58 --;
Line 32, change "T_1" to -- T_2 --; and change "58" to -- 68 --.

Column 8,
Line 43, after "first" insert -- gate --;
Line 44, after "second" insert -- gate --.

In Sheet 1 of the drawings, FIG._1, element 40 should show a PMOS symbol and element 42 should show an NMOS symbol.
In Sheet 1 of the drawings, FIG._4 should appear as follows:



Signed and Sealed this

Fifth Day of August, 2003

JAMES E. ROGAN
Director of the United States Patent and Trademark Office